



# Low-Cost Microprocessor Supervisory Circuits with Battery Backup

## General Description

The MAX703/MAX704 microprocessor ( $\mu$ P) supervisory circuits reduce the complexity and number of components required for power-supply monitoring and battery control functions in  $\mu$ P systems. These devices significantly improve system reliability and accuracy compared to that obtained with separate ICs or discrete components.

The MAX703/MAX704 are available in 8-pin DIP and SO packages and provide four functions:

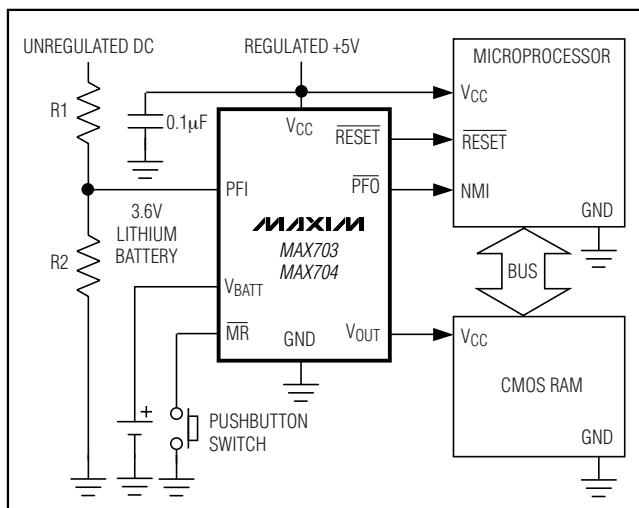
- 1) An active-low reset during power-up, power-down, and brownout conditions.
- 2) Battery-backup switching for CMOS RAM, CMOS  $\mu$ Ps, or other low-power logic circuitry.
- 3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
- 4) An active-low manual reset input.

The MAX703 and MAX704 differ only in their supply-voltage monitor levels. The MAX703 generates a reset when the supply drops below 4.65V, while the MAX704 generates a reset below 4.4V.

## Applications

Computers  
 Controllers  
 Intelligent Instruments  
 Automotive Systems  
 Critical  $\mu$ P Power Monitoring

## Typical Operating Circuit



## Features

- ◆ Battery-Backup Power Switching
- ◆ Precision Supply-Voltage Monitor  
4.65V (MAX703)  
4.40V (MAX704)
- ◆ 200ms Reset Pulse Width
- ◆ Debounced TTL/CMOS-Compatible Manual Reset Input
- ◆ 200 $\mu$ A Quiescent Current
- ◆ 50nA Quiescent Current in Battery-Backup Mode
- ◆ Voltage Monitor for Power-Fail or Low-Battery Warning
- ◆ 8-Pin DIP and SO Packages
- ◆ Guaranteed  $\overline{\text{RESET}}$  Assertion to  $V_{CC} = 1V$

## Ordering Information

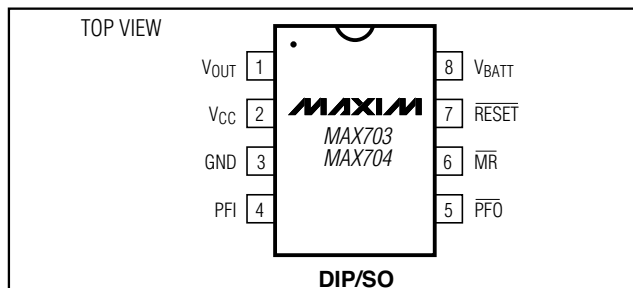
PART	TEMP RANGE	PIN-PACKAGE
MAX703C/D	0°C to +70°C	Dice*
MAX703CPA	0°C to +70°C	8 PDIP
MAX703CSA	0°C to +70°C	8 SO
MAX703EPA	-40°C to +85°C	8 PDIP
MAX703ESA	-40°C to +85°C	8 SO
MAX703MJA	-55°C to +125°C	8 CERDIP**
MAX704C/D	0°C to +70°C	Dice*
MAX704CPA	0°C to +70°C	8 PDIP
MAX704CSA	0°C to +70°C	8 SO
MAX704EPA	-40°C to +85°C	8 PDIP
MAX704ESA	-40°C to +85°C	8 SO
MAX704MJA	-55°C to +125°C	8 CERDIP**

\*Dice are tested at  $T_A = +25^\circ\text{C}$  only.

\*\*Contact factory for availability and processing to MIL-STD-883.

Devices in PDIP and SO packages are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering. Lead free not available for CERDIP package.

## Pin Configuration



MAX703/MAX704

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## ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)	Rate-of-Rise $V_{BATT}$ , $V_{CC}$ .....	100V/ $\mu$ s
$V_{CC}$ .....	-0.3V to +6.0V	
$V_{BATT}$ .....	-0.3V to +6.0V	
All Other Inputs (Note 1) .....	-0.3V to ( $V_{CB}$ + 0.3V)	
Input Current		
$V_{CC}$ .....	200mA	
$V_{BATT}$ .....	50mA	
GND .....	20mA	
Output Current		
$V_{OUT}$ .....	Short-Circuit Protected for Up to 10s	
All Other Outputs .....	20mA	
	Operating Temperature Range	
	C Suffix .....	0°C to +70°C
	E Suffix .....	-40°C to +85°C
	M Suffix .....	-55°C to +125°C
	Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )	
	8-Pin PDIP (derated 9.09mW/ $^\circ\text{C}$ above +70°C) .....	727mW
	8-Pin SO (derated 5.88mW/ $^\circ\text{C}$ above +70°C) .....	471mW
	8-Pin CERDIP (derated 8.00mW/ $^\circ\text{C}$ above +85°C) .....	640mW
	Storage Temperature Range .....	-65°C to +160°C
	Lead Temperature (soldering, 10s) .....	+300°C

**Note 1:**  $V_{CB}$  is the greater of  $V_{CC}$  and  $V_{BATT}$ . The input voltage limits on PFI and  $\overline{\text{MR}}$  may be exceeded if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{CC} = +4.75\text{V}$  to  $+5.5\text{V}$  for MAX703,  $V_{CC} = +4.5\text{V}$  to  $+5.5\text{V}$  for MAX704,  $V_{BATT} = 2.8\text{V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Operating Voltage Range $V_{CC}$ , $V_{BATT}$		(Note 2)	0		5.5	V	
Supply Current (Excluding $I_{OUT}$ )	$I_{SUPPLY}$	MAX70_C		200	350	$\mu\text{A}$	
		MAX70_E/M		200	500		
$I_{SUPPLY}$ in Battery-Backup Mode (Excluding $I_{OUT}$ )		$V_{CC} = 0\text{V}$ , $V_{BATT} = 2.8\text{V}$		0.05	1.0	$\mu\text{A}$	
		$T_A = +25^\circ\text{C}$			5.0		
$V_{BATT}$ Standby Current (Note 3)		$5.5\text{V} > V_{CC} > V_{BATT} + 0.2\text{V}$		-0.10	+0.02	$\mu\text{A}$	
		$T_A = T_{MIN}$ to $T_{MAX}$		-1.00	+0.02		
$V_{OUT}$ Output		$I_{OUT} = 5\text{mA}$	$V_{CC} - 0.05$	$V_{CC} - 0.025$		V	
		$I_{OUT} = 50\text{mA}$	$V_{CC} - 0.5$	$V_{CC} - 0.25$			
$V_{OUT}$ in Battery-Backup Mode		$I_{OUT} = 250\mu\text{A}$ , $V_{CC} < V_{BATT} - 0.2\text{V}$	$V_{BATT} - 0.1$	$V_{BATT} - 0.02$		V	
Battery Switch Threshold ( $V_{CC} - V_{BATT}$ )		$V_{CC} < V_{RST}$		20		mV	
				-20			
Battery Switchover Hysteresis				40		mV	
$\overline{\text{RESET}}$ Threshold	$V_{RST}$	MAX703	4.50	4.65	4.75	V	
		MAX704	4.25	4.40	4.50		
$\overline{\text{RESET}}$ Threshold Hysteresis				40		mV	
$\overline{\text{RESET}}$ Pulse Width	$t_{RST}$		140	200	280	ms	
$\overline{\text{RESET}}$ Output Voltage	$V_{OH}$	$I_{SOURCE} = 800\mu\text{A}$	$V_{CC} - 1.5$			V	
	$V_{OL}$	$I_{SINK} = 3.2\text{mA}$			0.4		
		MAX70_C, $V_{CC} = 1\text{V}$ , $V_{CC}$ falling, $V_{BATT} = 0\text{V}$ , $I_{SINK} = 50\mu\text{A}$					0.3
		MAX70_E/M, $V_{CC} = 1.2\text{V}$ , $V_{CC}$ falling, $V_{BATT} = 0\text{V}$ , $I_{SINK} = 100\mu\text{A}$					0.3

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +4.75V$  to  $+5.5V$  for MAX703,  $V_{CC} = +4.5V$  to  $+5.5V$  for MAX704,  $V_{BATT} = 2.8V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

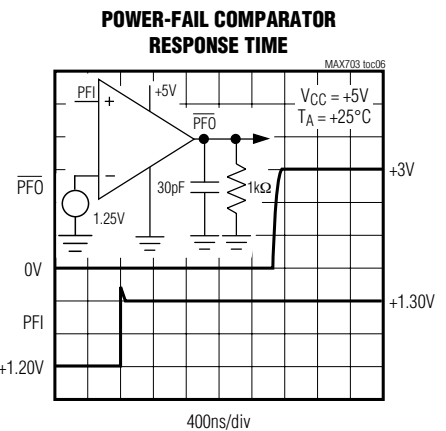
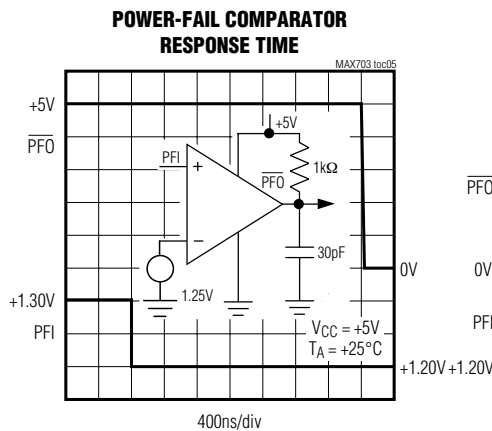
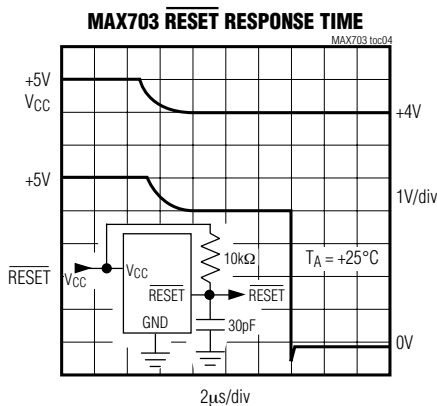
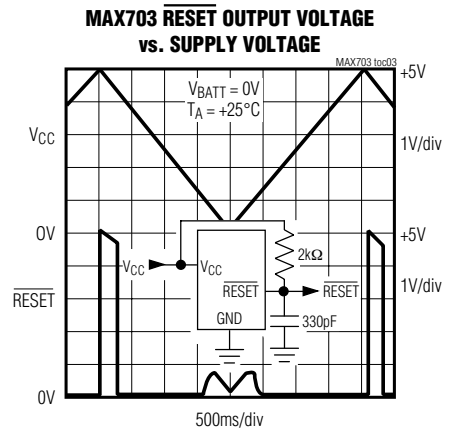
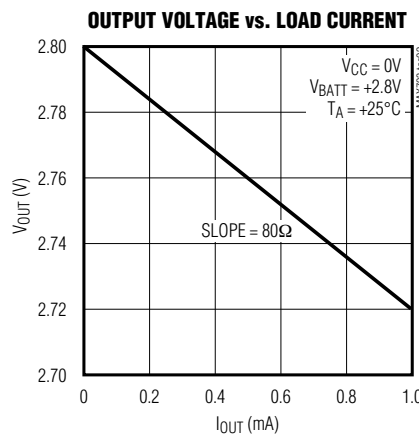
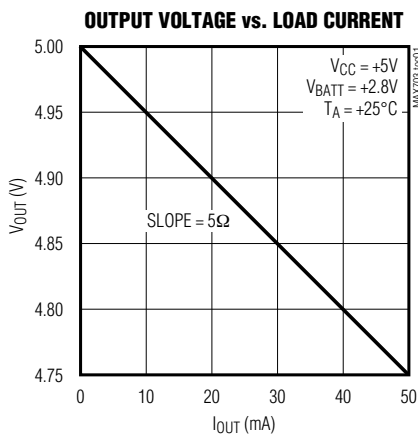
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{MR}$ Input Threshold	$V_{IL}$	Low			0.8	V
	$V_{IH}$	High	2.0			
$\overline{MR}$ Pulse Width	$t_{MR}$		150			ns
$\overline{MR}$ to RESET Delay	$t_{MD}$				250	ns
$\overline{MR}$ Pullup Current		$\overline{MR} = 0V$	100	250	600	$\mu A$
PFI Input Threshold		$V_{CC} = 5V$	1.20	1.25	1.30	V
PFI Input Current			-25	+0.01	+25	nA
$\overline{PFO}$ Output Voltage	$V_{OH}$	$I_{SOURCE} = 800\mu A$	$V_{CC} - 1.5$			V
	$V_{OL}$	$I_{SINK} = 3.2mA$	0.4			

**Note 2:** Either  $V_{CC}$  or  $V_{BATT}$  can go to 0V if the other is greater than 2.0V.

**Note 3:** “-” = battery-charging current, “+” = battery-discharging current.

## Typical Operating Characteristics

( $V_{CC} = +5V$ ,  $V_{BATT} = 2.8V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



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## Pin Description

PIN	NAME	FUNCTION
1	V <sub>OUT</sub>	Supply Output for CMOS RAM. When V <sub>CC</sub> is above the reset threshold, V <sub>OUT</sub> connects to V <sub>CC</sub> through a p-channel MOSFET switch. When V <sub>CC</sub> is below the reset threshold, the higher of V <sub>CC</sub> or V <sub>BATT</sub> is connected to V <sub>OUT</sub> .
2	V <sub>CC</sub>	+5V Supply Input
3	GND	Ground
4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low; otherwise $\overline{\text{PFO}}$ remains high. Connect PFI to GND or V <sub>CC</sub> when not used.
5	$\overline{\text{PFO}}$	Power-Fail Comparator Output. It goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{\text{PFO}}$ remains high.
6	$\overline{\text{MR}}$	Manual Reset Input. Generates a reset pulse when pulled below 0.8V. This active-low input is TTL/CMOS compatible and can be shorted to ground with a switch. It has an internal 250 $\mu$ A pullup current. Leave floating when not used.
7	$\overline{\text{RESET}}$	Reset Output. Remains low while V <sub>CC</sub> is below the reset threshold (4.65V for the MAX703, 4.40V for the MAX704). It remains low for 200ms after V <sub>CC</sub> rises above the reset threshold (Figure 2) or $\overline{\text{MR}}$ goes from low to high.
8	V <sub>BATT</sub>	Backup-Battery Input. When V <sub>CC</sub> falls below the reset threshold, V <sub>BATT</sub> is switched to V <sub>OUT</sub> if V <sub>BATT</sub> is 20mV greater than V <sub>CC</sub> . When V <sub>CC</sub> rises 20mV above V <sub>BATT</sub> , V <sub>CC</sub> is switched to V <sub>OUT</sub> . The 40mV hysteresis prevents repeated switching if V <sub>CC</sub> falls slowly.

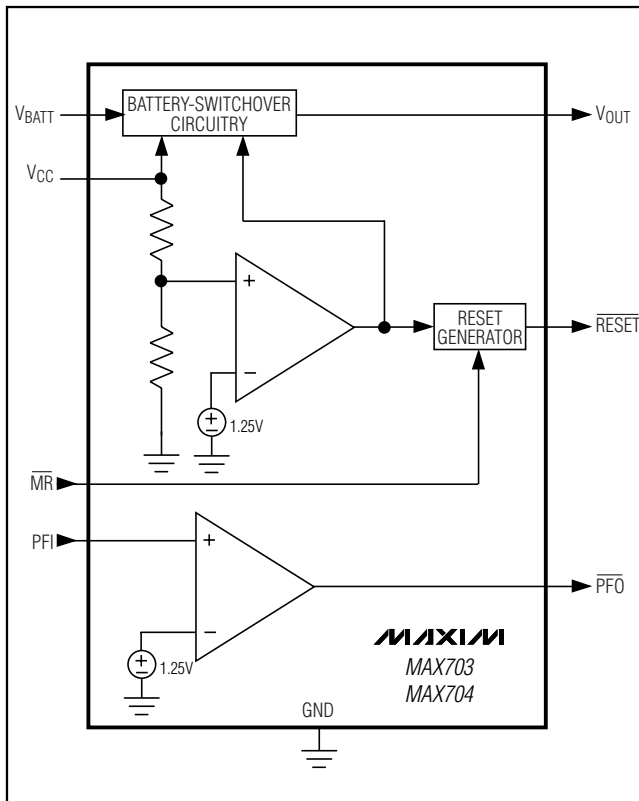


Figure 1. Block Diagram

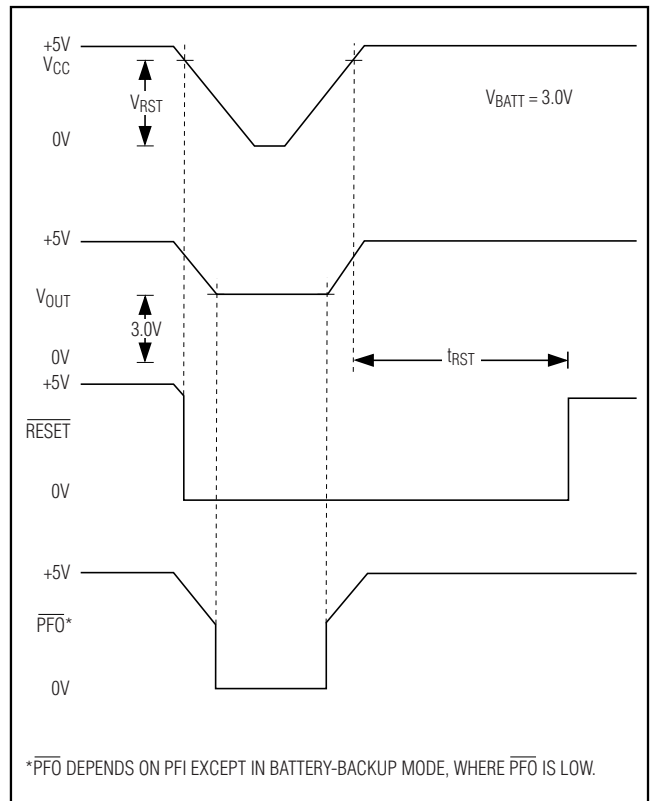


Figure 2. Timing Diagram

# Low-Cost Microprocessor Supervisory Circuits with Battery Backup

## Detailed Description

### RESET Output

A  $\mu\text{P}$ 's reset input starts the  $\mu\text{P}$  in a known state. Whenever the  $\mu\text{P}$  is in an unknown state, it should be held in reset. The MAX703/MAX704 assert reset when  $V_{CC}$  is low, preventing code-execution errors during power-up, power-down, or brownout conditions.

When  $V_{BATT}$  is 2V or more,  $\overline{\text{RESET}}$  is always valid, irrespective of  $V_{CC}$ . On power-up, as  $V_{CC}$  rises,  $\overline{\text{RESET}}$  remains low. When  $V_{CC}$  exceeds the reset threshold, an internal timer holds  $\overline{\text{RESET}}$  low for a time equal to the reset pulse width (typically 200ms); after this interval,  $\overline{\text{RESET}}$  goes high (Figure 2). If a power-fail or brownout condition occurs (i.e.,  $V_{CC}$  drops below the reset threshold),  $\overline{\text{RESET}}$  is asserted. As long as  $V_{CC}$  remains below the reset threshold, the internal timer is continually restarted, causing the  $\overline{\text{RESET}}$  output to remain low. Thus, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the end of the last interruption.

### Power-Fail Comparator

The PFI input is compared to an internal reference. If PFI is less than 1.25V,  $\overline{\text{PFO}}$  goes low. The power-fail comparator can be used as an undervoltage detector to signal a failing power supply. In the *Typical Operating Circuit*, an external voltage-divider at PFI is used to monitor the unregulated DC voltage from which the regulated +5V supply is derived.

The voltage-divider can be chosen so the voltage at PFI falls below 1.25V just before the +5V regulator drops out.  $\overline{\text{PFO}}$  is then used as an interrupt to prepare the  $\mu\text{P}$  for power-down.

To conserve power, the power-fail comparator is turned off and  $\overline{\text{PFO}}$  is forced low when the MAX703/MAX704 enter battery-backup mode.

### Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at  $V_{BATT}$ , the MAX703/MAX704 automatically switch RAM to backup power when  $V_{CC}$  fails.

As long as  $V_{CC}$  exceeds the reset threshold,  $V_{CC}$  connects to  $V_{OUT}$  through a  $5\Omega$  p-channel MOSFET power switch. Once  $V_{CC}$  falls below the reset threshold,  $\overline{\text{RESET}}$  goes low and  $V_{CC}$  or  $V_{BATT}$  (whichever is higher) switches to  $V_{OUT}$ . Note that  $V_{BATT}$  switches to  $V_{OUT}$  through an  $80\Omega$  switch) only if  $V_{CC}$  is below the reset-threshold voltage and  $V_{BATT}$  is greater than  $V_{CC}$ . When  $V_{CC}$  exceeds the reset threshold, it is connected to the MAX703/MAX704 substrate, regardless of the voltage

applied to  $V_{BATT}$  (Figure 3). During this time, diode D1 (between  $V_{BATT}$  and the substrate) conducts current from  $V_{BATT}$  to  $V_{CC}$  if  $V_{BATT} \geq (V_{CC} + 0.6\text{V})$ .

When the battery-backup mode is activated,  $V_{BATT}$  connects to  $V_{OUT}$ . In this mode, the substrate connects to  $V_{BATT}$  and internal circuitry is powered from the battery (Figure 3). Table 1 shows the status of the MAX703/MAX704 inputs and outputs in battery-backup mode.

When  $V_{CC}$  is below, but within, 1V of  $V_{BATT}$ , the internal switchover comparator draws about  $30\mu\text{A}$ . Once  $V_{CC}$

**Table 1. Input and Output Status in Battery-Backup Mode**

SIGNAL	STATUS
$V_{CC}$	Disconnected from $V_{OUT}$ .
$V_{OUT}$	Connected to $V_{BATT}$ through an internal $80\Omega$ p-channel MOSFET switch.
$V_{BATT}$	Connected to $V_{OUT}$ . Supply current is $< 1\mu\text{A}$ when $V_{CC} < (V_{BATT} - 1\text{V})$ .
$\overline{\text{RESET}}$	Logic-low.
PFI	Power-fail comparator is disabled.
$\overline{\text{PFO}}$	Logic-low.
$\overline{\text{MR}}$	Disabled.

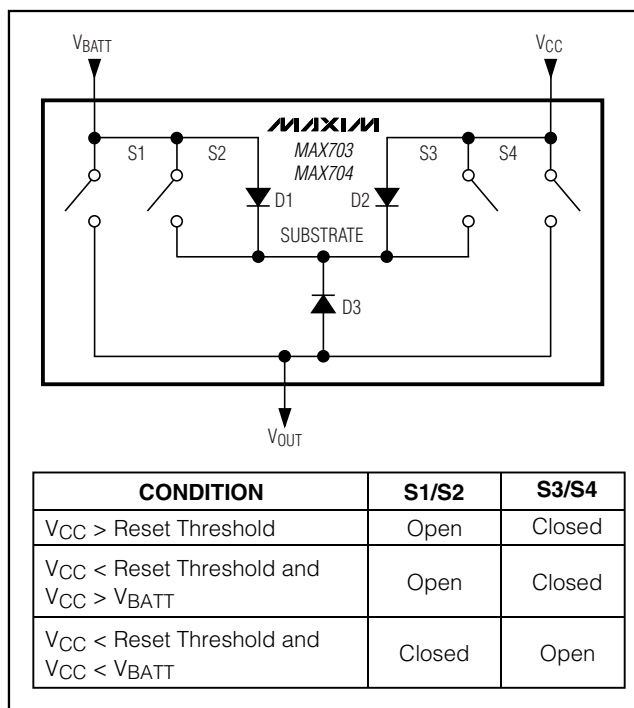


Figure 3. Battery-Switchover Block Diagram

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drops to more than 1V below  $V_{BATT}$ , the internal switchover comparator shuts off and the supply current falls to less than  $1\mu\text{A}$ .

## Manual Reset

The manual reset input ( $\overline{\text{MR}}$ ) allows  $\overline{\text{RESET}}$  to be activated by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. Because it is TTL/CMOS compatible,  $\overline{\text{MR}}$  can be driven by an external logic line.

## Applications Information

### Using a SuperCap® as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values (on the order of 0.1 Farad). When using SuperCaps, if  $V_{CC}$  exceeds the MAX703/MAX704 reset thresholds (4.65V and 4.40V, respectively),  $V_{BATT}$  may not exceed  $V_{CC}$  by more than 0.6V. Thus, with a 5% tolerance on  $V_{CC}$ ,  $V_{BATT}$  should not exceed  $V_{CC}(\text{min}) + 0.6\text{V} = 5.35\text{V}$ . Similarly, with a 10% tolerance on  $V_{CC}$ ,  $V_{BATT}$  should not exceed 5.1V.

Figure 4's SuperCap circuit uses the MAX703 with a  $\pm 5\%$  tolerance voltage supply. In this circuit, the SuperCap rapidly charges to within a diode drop of  $V_{CC}$ . However, the diode leakage current with trickle-charge the SuperCap voltage to  $V_{CC}$ . If  $V_{BATT} = 5.25\text{V}$  and the power is suddenly removed and then reapplied with  $V_{CC} = 4.75\text{V}$ ,  $V_{BATT} - V_{CC}$  does not exceed the allowable 0.6V difference voltage.

Figure 5's circuit uses the MAX704 with a  $\pm 10\%$  tolerance voltage supply. Note that if  $V_{CC} = 5.5\text{V}$  and  $V_{BATT} \leq 5.1\text{V}$ , the power can be suddenly removed and reapplied with  $V_{CC} = 4.5\text{V}$ , and  $V_{BATT} - V_{CC}$  will not exceed the allowable 0.6V voltage difference.

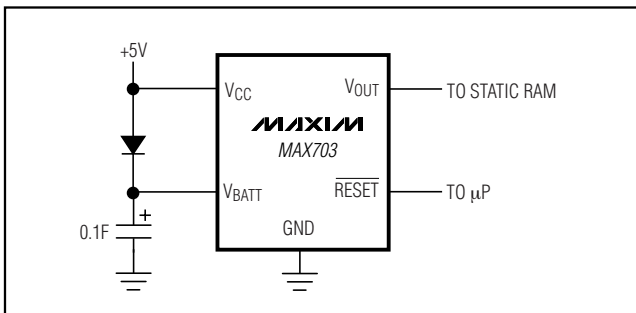


Figure 4. Using a SuperCap as a Backup Power Source with a MAX703 and a  $+5\text{V} \pm 5\%$  Supply

SuperCap is a registered trademark of Bankor Industries.

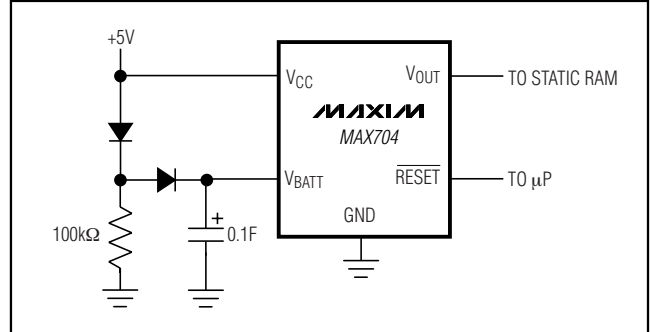


Figure 5. Using a SuperCap as a Backup Power Source with the MAX704 and a  $+5\text{V} \pm 10\%$  Supply

### Batteries and Power Supplies as Backup Power Sources

Lithium batteries work well as backup batteries because they have very low self-discharge rates and high-energy density. Single lithium batteries with open-circuit voltages of 3.0V to 3.6V are ideal for use with the MAX703/MAX704. Batteries with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be directly connected to the MAX703/MAX704  $V_{BATT}$  input with no additional circuitry (see the *Typical Operating Circuit*).

However, batteries with open-circuit voltages greater than the reset threshold plus 0.3V CANNOT be used as backup batteries, since they source current into the substrate through diode D1 (Figure 3) when  $V_{CC}$  is close to the reset threshold.

PART	MAXIMUM BACKUP-BATTERY VOLTAGE (V)
MAX703	4.80
MAX704	4.55

### Using the MAX703/MAX704 without a Backup Power Source

If a backup power source is not used, ground  $V_{BATT}$  and connect  $V_{CC}$  to  $V_{OUT}$ . A direct connection to  $V_{CC}$  eliminates any voltage drop across the internal switch, which would otherwise appear at  $V_{OUT}$ . Alternatively, use the MAX705–MAX708, which do not have battery-backup capabilities.

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## Ensuring a Valid RESET Output Down to VCC = 0V

When VCC falls below 1V, the MAX703/MAX704 RESET output no longer sinks current; it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left as open circuits. If a pull-down resistor is added to the RESET pin as shown in Figure 6, any stray charge or leakage currents will flow to ground, holding RESET low. Resistor value R1 is not critical. It should be about 100kΩ, which is large enough not to load RESET and small enough to pull RESET to ground.

## Replacing the Backup Battery

The backup battery can be removed while VCC remains valid without triggering a reset. As long as VCC stays above the reset threshold, battery-backup mode cannot

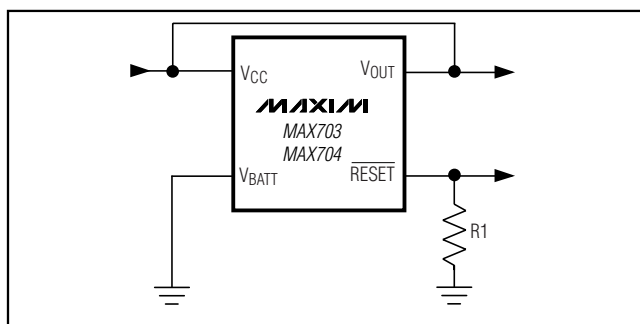


Figure 6. RESET Valid to Ground Circuit

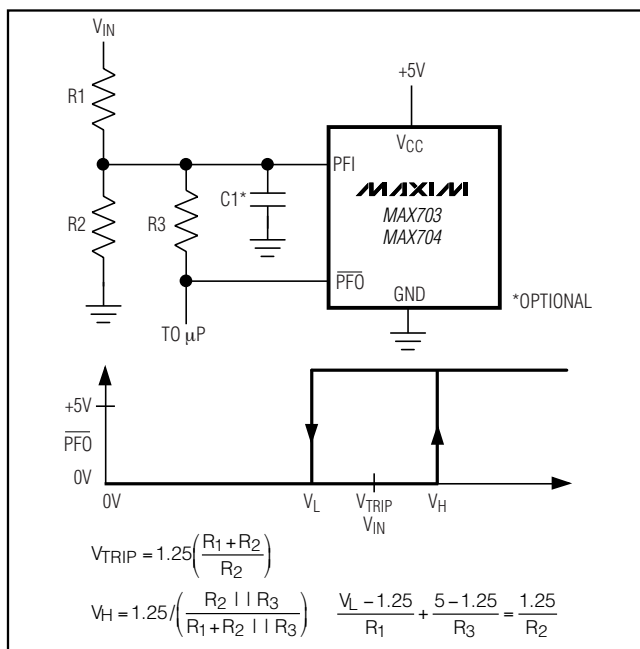


Figure 7. Adding Hysteresis to the Power-Fail Comparator

be entered. This is an improvement on switchover ICs that initiate a reset when VCC and VBATT are at or near the same voltage level (regardless of the reset threshold voltage). If the voltage on the unconnected VBATT pin floats up toward VCC, this condition alone cannot initiate a reset when using the MAX703/MAX704.

## Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when VIN is near the power-fail comparator trip point. Figure 7 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 so that PFI sees 1.25V when VIN falls to the desired trip point (VTRIP). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1μA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the PFO pin. Capacitor C1 adds additional noise rejection.

## Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 8's circuit. When the negative supply is valid, PFO is low. When the negative supply voltage droops, PFO goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the VCC voltage, and resistors R1 and R2.

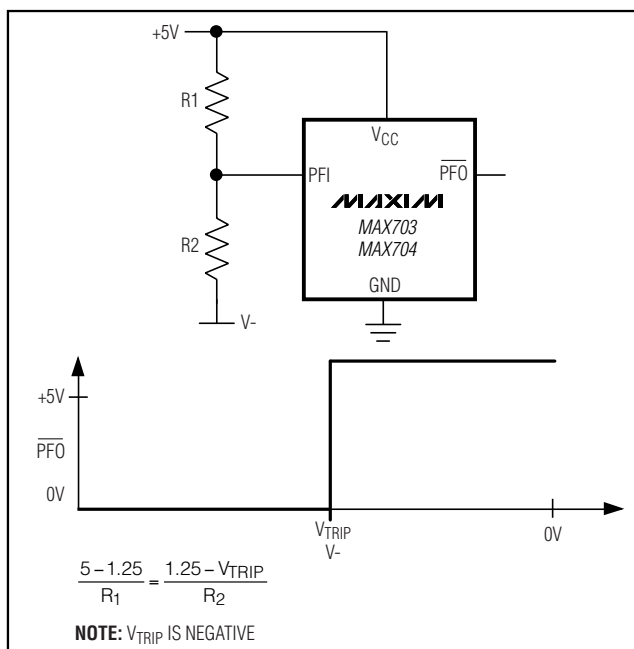


Figure 8. Monitoring a Negative Voltage

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## Using the Power-Fail Comparator to Assert Reset

In addition to asserting reset at the V<sub>CC</sub> reset threshold voltage, reset can also be asserted at the PFI input threshold voltage. Connect PFO to MR to initiate a reset

pulse when the monitored supply drops below a user-specified threshold or when V<sub>CC</sub> falls below the reset threshold. For additional noise rejection, place a capacitor between PFI and GND.

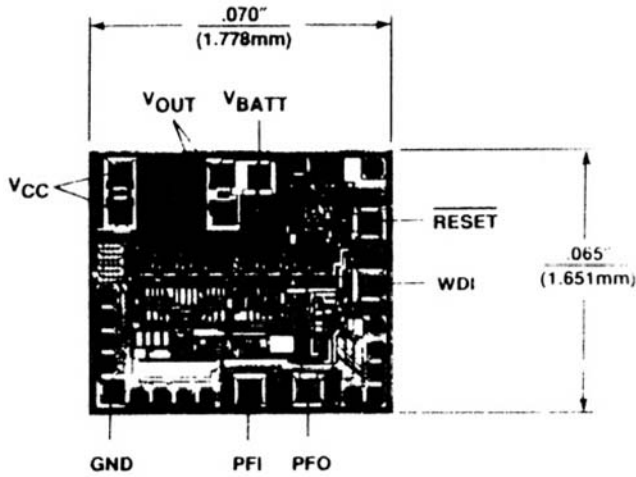
**Table 3. Maxim Microprocessor Supervisory Products**

PART	NOMINAL RESET THRESHOLD (V)	MINIMUM RESET PULSE WIDTH (ms)	NOMINAL WATCH-DOG TIMEOUT PERIOD (s)	BACKUP-BATTERY SWITCH	$\overline{CE}$ WRITE PROTECT	POWER-FAIL COMPARATOR	MANUAL RESET INPUT	WATCH-DOG INPUT	LOW-LINE OUTPUT	ACTIVE-HIGH RESET	BATT ON OUTPUT
MAX690A	4.65	140	1.6	Yes	No	Yes	No	No	No	No	No
MAX691A	4.65	140/Adj.	1.6/Adj.	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
MAX692A	4.40	140	1.6	Yes	No	Yes	No	No	No	No	No
MAX693A	4.40	140/Adj.	1.6/Adj.	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
MAX696	Adj.	35/Adj.	1.6/Adj.	Yes	No	Yes	No	Yes	Yes	Yes	Yes
MAX697	Adj.	35/Adj.	1.6/Adj.	No	Yes	Yes	No	Yes	Yes	Yes	No
MAX700	4.65/Adj.	200	—	No	No	No	Yes	No	No	Yes	No
MAX703	4.65	140	—	Yes	No	Yes	Yes	No	No	No	No
MAX704	4.40	140	—	Yes	No	Yes	Yes	No	No	No	No
MAX705	4.65	140	1.6	No	No	Yes	Yes	Yes	No	No	No
MAX706	4.40	140	1.6	No	No	Yes	Yes	Yes	No	No	No
MAX707	4.65	140	—	No	No	Yes	Yes	No	No	Yes	No
MAX708	4.40	140	—	No	No	Yes	Yes	No	No	Yes	No
MAX791	4.65	140	1.0	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MAX1232	4.50/4.75	250	0.15/0.60/ 1.2	No	No	No	Yes	No	No	Yes	No
MAX1259	—	—	—	Yes	No	Yes	No	No	No	No	No



# Low-Cost Microprocessor Supervisory Circuits with Battery Backup

## Chip Topography



## Package Information

For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

MAX703/MAX704

SUBSTRATE MUST BE LEFT UNCONNECTED  
TRANSISTOR COUNT: 573

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